ABSTRACT OF THE DISCLOSURE

Memory apparatus including a byte-bank organized in N rows and 8 columns, having a capacity of $\log_2(N)$ bytes, a $\log_2(N)$ bit address bus operative to address the byte-bank, an address offset bus operative to generate offsets (e.g., one-bit offsets) to bits of the byte-bank with an address conversion operator, and an adder in operative communication with the address offset bus and the $\log_2(N)$ bit address bus, the adder operative to add addresses of the byte-bank with the offset generated by the address conversion operator and output a result to the $\log_2(N)$ bit address. A random access memory array may include a plurality of the byte-banks.